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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/382,929	08/25/1999	PAUL A. FARRAR	303.603US1	5871

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/382,929	FARRAR, PAUL A.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-10,12,14,15,18-23,31-36,38-46 and 75-94* is/are pending in the application.

4a) Of the above claim(s) *15,18-23,31-36,38-46 and 75-93* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10,12,14 and 94* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10-16-6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 6, 8-10, 12 and 14 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chiang (6040628).

At column 2, line 55 to column 3, line 26; and column 8, lines 29-41, Chiang discloses the following:

Re claim 6: An integrated circuit assembly comprising: an electronic substrate 100; and a conductive structure 130, 170 embedded in a plurality of materials 140, 195 each of the plurality of materials inherently having a different vaporization temperature, the plurality of materials is formed on the electronic substrate and the conductive structure is coupled to the electronic substrate; wherein each of the plurality of materials contacts (at least thermally) a surface of the electronic substrate.

Re claim 8: The integrated circuit assembly of claim 6, wherein at least one of the plurality of materials 195 is silicon dioxide.

Re claim 9: The integrated circuit assembly of claim 6, wherein at least one of the plurality of materials is carbon 140 "organic."

Re claim 10: An integrated circuit assembly comprising: an electronic substrate 100; and a conductive structure embedded in a material layer having a structural component 195 inherently having a structural vaporization temperature and a fill material 140 having a vaporization temperature inherently less than the structural vaporization temperature, the material layer is formed on the electronic substrate and the conductive structure is coupled to the electronic substrate, wherein the conductive structure includes a horizontal conductive interconnect 170 formed in and above the fill material and at least one vertical wiring via 130 coupling the horizontal conductive interconnect to the electronic substrate.

Re claim 12: The integrated circuit assembly of claim 10, wherein the structural component having a structural vaporization temperature is fabricated from silicon dioxide.

Re claim 14: The integrated circuit assembly of claim 10, wherein the fill material is fabricated from carbon "organic."

To further clarify the disclosure of a structural component 195 inherently having a structural vaporization temperature and a fill material

140 having a vaporization temperature inherently less than the structural vaporization temperature, these are inherent properties of the materials of 140 and 195. Indeed, it is these properties that enable the process of Chiang, "a hard mask 180 made of silicon dioxide 195 and silicon nitride 190, to enable lithographic patterning and plasma etching [vaporization] of organic polymer 140 to create vias 160."

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 94 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Chiang (6040628) and Tobita (5801412).

Chiang is applied for the same reasons it is applied to the rejection of claims 6, 8-10, 12 and 14.

In addition, Chiang discloses the following:

Re claim 1: An integrated circuit assembly comprising: an electronic chip substrate 100; and a conductive structure 130, 170 embedded in a material layer 140, 195 inherently having a plurality of vaporization temperatures, the material layer is formed on the electronic substrate and

the conductive structure includes a horizontal conductive interconnect 130 and at least one vertical wiring via 170 coupling the horizontal conductive interconnect to the electronic substrate, wherein the horizontal conductive interconnect is formed in and above a fill material 140.

Re claim 4: The integrated circuit assembly of claim 1, wherein the conductive structure is fabricated from "copper."

However, Chiang does not appear to explicitly disclose the following:

Re claim 1: An electronic chip.

Re claim 2: The integrated circuit assembly of claim 1, wherein the electronic substrate is a memory substrate.

Re claim 3: The integrated circuit assembly of claim 2, wherein the memory substrate is a dynamic random access memory substrate.

Nevertheless, in the abstract, and at column 13, lines 5-41; column 25, lines 44-58; and column 26, lines 36-52, Tobita discloses an electronic "chip"; wherein an electronic substrate 1 is a memory substrate; wherein the memory substrate is a dynamic random access memory substrate. Furthermore, it would have been obvious to combine this disclosure of Tobita with the disclosure of Chiang because it would facilitate provision of the electronic substrate of Chiang, and, as disclosed by Tobita, having excellent area efficiency, and it would provide the chip of Tobita with an interconnect

structure, having, as disclosed by Chiang, a low dielectric constant material for insulation having advantages and desirable for reducing capacitance.

However, Chiang and Tobita does not appear to explicitly disclose the following:

Re claim 94: The integrated circuit assembly of claim 1, wherein the electronic chip is a flip chip.

Regardless, the combination of Chiang and Tobita inherently discloses a flip chip because the term "flip" merely limits the scope of the term "chip" to an intended use of the chip and does not appear to result in a structural difference between the claimed chip and the chip of the applied prior art. Further, because the chip of Chiang and Tobita appears to have the same structure as the claimed chip, it appears to be capable of being used for the intended use, and the intended use does not patentably distinguish the claimed chip from the chip of Chiang and Tobita. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And,

"Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang as applied to claim 1, and further in combination with Jeng (5923074).

As cited supra, Chiang discloses the following:

Re claim 5: The integrated circuit assembly of claim 1, An integrated circuit assembly comprising: an electronic substrate; and a conductive structure embedded in a material layer inherently having a plurality of vaporization temperatures, the material layer is formed on the electronic substrate and the conductive structure includes a horizontal conductive interconnect and at least one vertical wiring via coupling the horizontal conductive interconnect to the electronic substrate, wherein the horizontal conductive interconnect is formed in and above a fill material.

However, Chiang does not appear to explicitly disclose the following

Re claim 5: Wherein at least one of the plurality of vaporization temperatures is about 400 degrees centigrade.

Still, Chiang discloses a low dielectric organic polymer. In addition, at column 1, line 63 to column 2, line 20; column 2, lines 44-61; column 4, lines 7-23; column 4, line 48 to column 5, line 5; column 6, lines 31-33; column 6, line 65 to column 7, line 4; column 7, lines 26-33; and column 8, lines 24-31, Jeng discloses wherein a vaporization temperature of a low dielectric organic polymer "parylene" is about 400 degrees centigrade. Bertin (5702984), at column 11, lines 50-51, further evidences this inherent property of parylene. Furthermore, it would have been obvious to combine this disclosure of Jeng with the disclosure of Chiang because it would facilitate provision of the low dielectric organic polymer of Chiang.

In the alternative, claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang and Tobita as applied to claim 1, and further in combination with Jeng (5923074).

Chiang and Tobita do not appear to explicitly disclose the following:

Re claim 94: The integrated circuit assembly of claim 1, wherein the electronic chip is a flip chip.

Notwithstanding, at column 1, lines 44-55, Jeng disclose wherein an electronic chip is a "flip-chip." In addition, it would have been obvious to combine this disclosure of Jeng with the disclosure of Chiang because, as

disclosed by Jeng, it would allow for a higher density of interconnections and simplify circuit layout.

Applicant's remarks filed 10-16-6 have been fully considered and are deemed moot in view of the new grounds of rejection.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
25-May-07